CLAIMS:

1. A processing system comprising a plurality of processing elements, the plurality of processing elements comprising a first set of processing elements and at least a second set of processing elements,
wherein each processing element of the first set comprises a register file and at least one instruction issue slot, the instruction issue slot comprising at least one functional unit, and the processing element being arranged to execute instructions under a common thread of control,
wherein each processing element of the second set comprises a register file and a plurality of instruction issue slots, each instruction issue slot comprising at least one functional unit, and the processing element being arranged to execute instructions under a common thread of control,
and wherein the number of instruction issue slots in the processing elements of the second set is substantially higher than the number of instruction issue slots in the processing elements of the first set,
and wherein the processing system further comprises inter-processor communication means arranged for communicating between processing elements of the plurality of processing elements.

2. A processing system according to claim 1, characterized in that the processing elements of the plurality of processing elements are arranged in a network, wherein a processing element of the first set is arranged for direct communication with a processing element of only the second set, via the inter-processor communication means,
and wherein a processing element of the second set is arranged for direct communication with a processing element of only the first set, via the inter-processor communication means.

3. A processing system according to claim 1, characterized in that the plurality of issue slots organized in a processing element of the second set of processing elements share at least one common control signal for controlling instruction execution.

4. A processing system according to claim 1, characterized in that the processing elements of the first set of processing elements are arranged for issuing only one operation per cycle.

5. A processing system according to claim 1, characterized in that the processing elements of the second set of processing elements are Very Large Instruction Word processors, wherein the register file is accessible for said processing elements by the corresponding functional units and wherein the processing elements further comprise a local communication network for coupling the register file and the corresponding functional units.

6. A processing system according to claim 1, characterized in that the processing elements of the first set of processing elements are Very Large Instruction Word processors, wherein the register file is accessible for said processing elements by the corresponding functional units and wherein the processing elements further comprise a local communication network for coupling the register file and the corresponding functional units.

7. A processing system according to claim 5 or 6, characterized in that the register file corresponding to a processing element is a distributed register file.

8. A processing system according to claim 5 or 6, characterized in that the local communication network corresponding to a processing element is a partially connected communication network.

9. A processing system according to claim 1, characterized in that the inter-processor communication means comprise a data-driven synchronized communication means.

10. A processing system according to claim 9, characterized in that the data-driven synchronized communication means comprise a blocking First-In-First-Out buffer.

11. A processing system according to claim 1, characterized in that the processing elements of the plurality of processing elements are arranged to be bypassed by the inter-processor communication means.

12. A method for programming a processing system, wherein the processing system comprises a plurality of processing elements, the plurality of processing elements comprising a first set of processing elements and at least a second set of processing elements, wherein each processing element of the first set comprises a register file and at least one instruction issue slot, the instruction issue slot comprising at least one functional unit, and the processing element being arranged to execute instructions under a common thread of control, wherein each processing element of the second set comprises a register file and a plurality of instruction issue slots, each instruction issue slot comprising at least one functional unit, and the processing element being arranged to execute instructions under a common thread of control,

and wherein the number of instruction issue slots in the processing elements of the second set is substantially higher than the number of instruction issue slots in the processing element of the first set,

and wherein the processing system further comprises inter-processor communication means arranged for communicating between processing elements of the plurality of processing elements,

and wherein the method of programming the processing system comprises the following steps:

- identifying a first set of functions in an application graph wherein each function inherently contains instructions to be executed mainly sequentially,
- identifying a second set of functions in an application graph wherein each function inherently contains instruction-level parallelism,
- mapping the first set of functions onto processing elements of the first set of processing elements,
- mapping the second set of functions onto processing elements of the second set of processing elements.

13. A method for programming a processing system according to claim 12, characterized in that the method further comprises the step of:

- bypassing a processing element of the plurality of processing elements by the inter-processor communication means.

14. A compiler program product being arranged for implementing all steps of the method for programming a processing system according to claim 12 or 13, when said compiler program product is run on a computer system.